Attorney's Docket No.: 07977/192001/US3444

REMARKS

Reconsideration and allowance of the above referenced application are respectfully requested.

Claims 61, 73-76, and 87 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over the admitted prior art in view of Kobeda and/or Sasaki. Claim 86 stands rejected over this combination and further in view of Tang. In response, the claims are amended in order to overcome these rejections. Each claim has been amended to include the further structure which is disclosed in figure 1F, specifically "a second layer comprising metal provided on said insulating surface and being in contact with the other one of said source region and drain region". This is supported by reference numeral 15A and Figure 1F. In addition, the claims are amended to recite "a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said layer comprising metal through said second contact hole". This is supported by reference numeral 17. In addition, the limitation of "wherein said first and second contact holes are located outside said source region, said drain region, and said first gate interconnection" is also supported in Figure 1F.

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The admitted prior art does not teach the first and second contact holes being located outside said source region, drain region and first gate interconnection.

Kobeda '702 does teach a contact hole outside the source or drain region and the gate interconnect in Figure 3. However, it appears that Kobeda '702 does not teach both the first and second contact holes being located outside the source region, drain region, and first gate interconnection as defined by the amended claims. In addition, it does not appear that these features are found in Sasaki '068 or in Tang '141.

This should obviate all of the remaining rejections, and therefore it is respectfully suggested that the claims should be in condition for allowance.

Please apply $110.00 for a one month extension and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/27/03

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Attached is a marked-up version of the changes being made by the current amendment.

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Version with markings to show changes made

In the claims:

In the pending claims, please amend claims 61, 73-76, 83, 85, 86, 87 and 95-101 as follows.

61. (Amended) A display device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, [and] said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric; [and]

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole[,]; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact [hole is] holes are located outside said source region, said drain region and said first gate interconnection.

73. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region, said first layer comprising metal being connected with said first gate interconnection through no contact hole;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, [and] said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric; [and]

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole[,]; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact [hole is] holes are located outside said source region, said drain region and said first gate interconnection.

74. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate

interconnection and being connected with one of said source region and said drain region;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric comprising silicon nitride provided over said gate electrode, [and] said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric; [and]

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole[,]; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact [hole is] holes are located outside said source region, said drain region and said first gate interconnection.

75. (Amended) A semiconductor device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric comprising silicon oxide provided over said gate electrode, [and] said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric; [and]

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole[,]; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact [hole is] holes are located outside said source region, said drain region and said first gate interconnection.

76.(Amended) A semiconductor device comprising:

a substrate having an insualting surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode comprising a doped polycrystalline silicon provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, [and] said first layer comprising metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising metal in said interlayer dielectric; [and]

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising metal through said first contact hole[,]; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact [hole is] holes are located outside said source region, said drain region and said first gate interconnection.

83. (Amended) The device of claim 75 wherein said first layer comprising metal is connected with said first gate interconnection through no contact hole.

85. (Amended) The device of claim 76 wherein said first layer comprising metal is connected with said first gate interconnection through no contact hole.

86. (Amended) A display device comprising:

a substrate having an insulating surface;

a semiconductor island comprising silicon provided over said insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising said metal provided on said insulating surface and being in direct contact with said first gate interconnection and being connected with one of said source region and said drain region;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, [and] said first layer comprising said metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising said metal in said interlayer dielectric; [and]

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising said metal through said first contact hole[,]; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact [hole is] holes are located outside said source region, said drain region and said first gate interconnection.

87. (Amended) A semiconductor device comprising:

a semiconductor island comprising silicon provided on an insulating surface;

a source region and a drain region provided in said semiconductor island, said source region and said drain region comprising a silicide of a metal;

a channel region provided in said semiconductor island between said source region and said drain region;

a gate electrode provided adjacent to said channel region with a gate insulating film therebetween;

a first gate interconnection formed on said insulating surface;

a first layer comprising said metal provided on said insulating surface and being in direct contact with said first interconnection and being connected with one of said source region and said drain region, said layer comprising said metal being connected with said gate interconnection through no contact hole;

a second layer comprising metal provided on said insulating surface and being in direct contact with the other one of said source region and said second region;

an interlayer dielectric provided over said gate electrode, [and] said first layer comprising said metal and said second layer comprising metal;

a first contact hole provided over said first layer comprising said metal in said interlayer dielectric; and

a second contact hole provided over said second layer comprising metal in said interlayer dielectric;

a second interconnection comprising aluminum provided over said interlayer dielectric and connected with said first layer comprising said metal through said first contact hole[,]; and

a third interconnection comprising aluminum provided over said interlayer dielectric and connected with said second layer comprising metal through said second contact hole,

wherein said first and second contact [hole is] holes are located outside said source region, said drain region and said first gate interconnection.

95. (Amended) A display device according to claim 61, wherein said first gate interconnection is provided in a same layer as said gate electrode.

96. (Amended) A semiconductor device according to claim 73, wherein said first gate interconnection is provided in a same layer as said gate electrode.

97. (Amended) A semiconductor device according to claim 74, wherein said first gate interconnection is provided in a same layer as said gate electrode.

98. (Amended) A semiconductor device according to claim 75, wherein said first gate interconnection is provided in a same layer as said gate electrode.

99. (Amended) A semiconductor device according to claim 76, wherein said first gate interconnection is provided in a same layer as said gate electrode.

100. (Amended) A display device according to claim 86, wherein said first gate interconnection is provided in a same layer as said gate electrode.

101. (Amended) A semiconductor device according to claim 87, wherein said first gate interconnection is provided in a same layer as said gate electrode.